You Wu

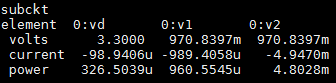
ECE 222

Lab 2: Current Mirror and Differential Amplifier

Part 1: Current Mirror

A current mirror was designed with Vout1 = Vout2 = Vdd = 3.3V, Vss = 0V, Iref = 100uA, Iout1 = 1mA, Iout2 = 5mA, Rout1 > 10k when Vout1 > 0.6V, Rout2 > 2k Vout2 > 0.6V. Vout1 and Vout2 were set to match Vdd to get an effective current ratio. . Plugging in μn = 460, Cox = 9.5nm, Iref = 100uA and setting (W/L) to 10, we get VGS0 = 1.046V and R = 22.5k.

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| Schematic | Netlist |
|  | \*\* Part 1 - Current Mirror - Output Voltage \*\*  .INCLUDE sedra\_lib.lib  \* DC and AC Sources  VD VDD 0 DC 3.3V  V1 D1 0 DC 1.0883V  V2 D2 0 DC 1.0883V  \* Resistors  R VDD D0 23.541K  \* MOSFETs  M0 D0 D0 0 0 NMOS0P5 W=5U L=0.5U  M1 D1 D0 0 0 NMOS0P5 W=50U L=0.5U  M2 D2 D0 0 0 NMOS0P5 W=250U L=0.5U  .OPTIONS POST  .OP  \*\* Part 1  .PROBE I(M0)  .PROBE I(M1)  .PROBE I(M2)  \*\* Finding the output resistance  .DC V1 0.1 3.3 0.01  .PRINT V(D1) I(M1)  .MEASURE DC I1a FIND I(M1) WHEN V(D1)=0.6  .MEASURE DC I1b FIND I(M1) WHEN V(D1)=3.3  .DC V2 0.1 3.3 0.01  .PRINT V(D2) I(M2)  .MEASURE DC I2a FIND I(M2) WHEN V(D2)=0.6  .MEASURE DC I2b FIND I(M2) WHEN V(D2)=3.3  \*\* Finding the output voltage  .DC V1 0.1 3.3 0.01  .MEASURE DC Vout1 FIND V(D1) WHEN I(M1)=1.00E-3  .DC V2 0.1 3.3 0.01  .MEASURE DC Vout2 FIND V(D2) WHEN I(M2)=5.00E-3  .END |



Iref was found to be 98.94uA, Iout1 was found to be 0.9894mA and Iout2 was found to be 4.947mA.

Using DC analysis, Rout was calculated using Vout sweep and the two current outputs.

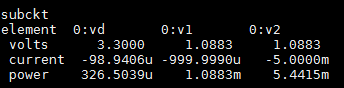
Using AC analysis, the small-signal resistance was computed to compare with Rout.



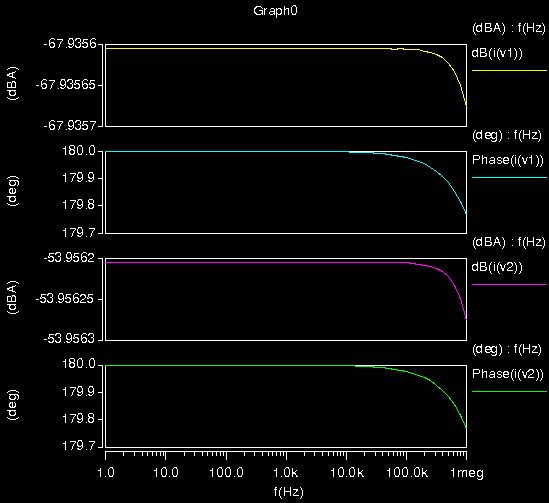
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| --- | --- |
| Part 2: DC Analysis | Part 3: AC Analysis |
| \*\* Part 1 - Current Mirror - DC Analysis \*\*  .INCLUDE sedra\_lib.lib  \* DC and AC Supplies  VD VDD 0 DC 3.3V  V1 D1 0 DC 1.0883V  V2 D2 0 DC 1.0883V  .PARAM wx = 50U  \* Resistors  R VDD D0 23.541K  \* MOSFETs  M0 D0 D0 0 0 NMOS0P5 W=5U L=0.5U  M1 D1 D0 0 0 NMOS0P5 W=wx L=0.5U  M2 D2 D0 0 0 NMOS0P5 W=250U L=0.5U  \*\* Analysis Requests  .OPTIONS POST  .OP  .DC wx 1U 100U 10U  .PLOT DC I(M1) wx  .END | \*\* Part 1 - Current Mirror - AC Analysis \*\*  .INCLUDE sedra\_lib.lib  \* DC and AC Sources  VD VDD 0 DC 3.3V AC 1  V1 D1 0 DC 1.0883V  V2 D2 0 DC 1.0883V  \* Resistors  R VDD D0 23.541K  \* MOSFETs  M0 D0 D0 0 0 NMOS0P5 W=5U L=0.5U  M1 D1 D0 0 0 NMOS0P5 W=50U L=0.5U  M2 D2 D0 0 0 NMOS0P5 W=250U L=0.5U  \*\* AC Analysis  .OPTIONS POST  .OP  .AC DEC 10 1 1E6  .END |

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| Vout > 0.6 V, ΔV = 2.7 V | Vout > 0.6 V, ΔV = 2.7 V |
| ΔI = 0.24354mA | ΔI = 1.2175mA |
| Rout1 = 11.09 KΩ > 10 KΩ | Rout2 = 2.22 KΩ > 2 KΩ |
|  |  |
| Vout1 = 1.088V | Vout2 = 1.088V |

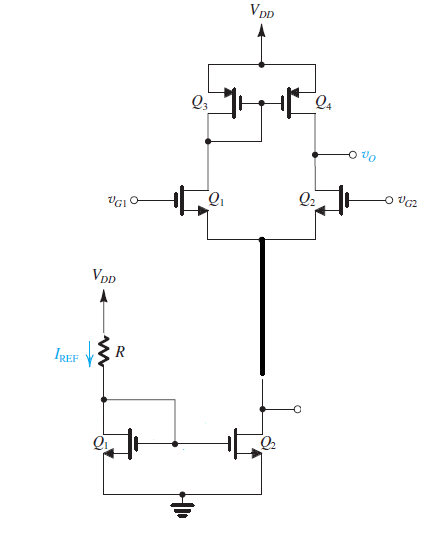
Overall, the initial design meets the specifications listed.



The early voltage is computed with 1/λ = 10 V. ro1 = 10kΩ and ro2 = 2kΩ which is approximately equivalent to the values of Rout1 and Rout2 computed above.

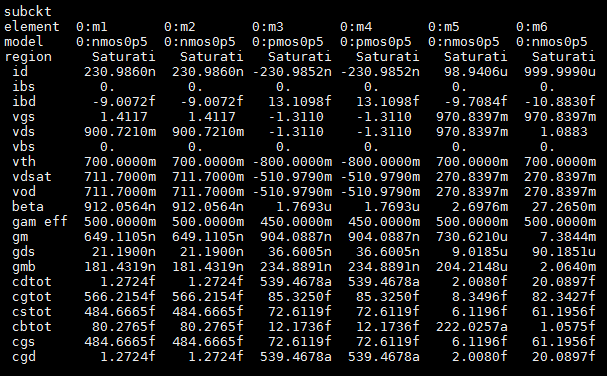


Part 2: Active-Loaded differential Amplifier

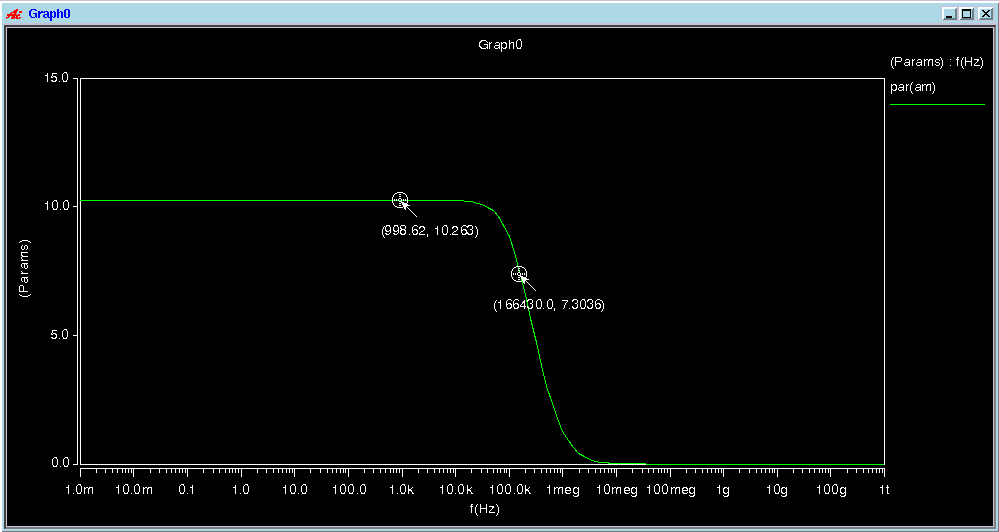


The schematic above was built using portions of the current mirror netlist. Cl was set at 0.2pF, Vdd = 3.3V, Vss = 0V, I = 1mA, Am > 10, BW3dB = fH, and the total gate width < 1000um.

The gain can be rewritten as A = VA/(VGS-VT) = 10 V/V, so VGS = 1.7 V. Therefore, using leads to W/L = 1/20 for the NMOS transistors and W/L = 1/30 for PMOS transistors.



Both VG1 and VG2 bias voltages were set to 2.5V so their differential voltage is 0V. The transistors are operating in the pinch-off region.



The differential gain is 10.263 and the 3db frequency of the transistors is approximately 166kHz.

Gain-bandwidth product (GB) is constant which means you can trade off gain for increased bandwidth.